UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,197	01/28/2004	Douglas L. Youngblood	INSL.0083	3357

26122 7590 01/24/2008

LAW OFFICES OF GARY R. STANFORD
330 W OVERLOOK MOUNTAIN RD
BUDA, TX 78610

EXAMINER	
LAO, LUN YI	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
01/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,197	YOUNGBLOOD ET AL.	
	Examiner	Art Unit	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-15 and 17-22* is/are rejected.

7)☒ Claim(s) *5-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 9-13 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo et al(7,023,458) in view of Kato(US 20020126112).

As to claims 1, 9-13 and 18-22, Kudo et al each a gamma correction circuit comprising: a resistor ladder(307 or 1202)(see figures 3, 12, 13; column 7, lines 44-59; column 17, lines 18-59 and column 18, lines 5-52) coupled to a reference voltage(316); a plurality of adjustable resistors distributed along the resistor ladder and providing a plurality of selectable tap voltages(see figures 3, 7, 12, 13 and column 7, lines 44-59)), wherein the resistor ladder(307 or 1202) comprising a plurality of first resistors(326-330) coupled in series, each of the plurality of the first resistors(326-330) having a plurality of second resistors(308-313) coupled in series forming a plurality intermediate location(see figure 7); a programmable non-volatile memory that stores at least one digital gamma value(see figures 3, 9, 12-16; column 7, lines 30-43; column 15, lines 7-68 and column 16, lines 1-12); select logic(304-306, 308-313 or 1204, 1205 or 1301-1306) which inserts each of the adjustable resistors into the resistor ladder(307, 1202)

into M of the plurality of first resistors(326-330) by inserting a corresponding one of the M adjustable tap resistors at a selected one of the plurality of intermediate locations of a corresponding one of the plurality of first resistors(326-330), and selecting a point of each of the adjustable resistor to select each of M tap voltages based on the digital information stored in the memory, coupled to the memory and to the plurality of adjustable resistors, that selects each of the selectable voltages according to the at least one digital gamma value(see figures 3, 12-13; column 7, lines 44-68; column 8; column 17, lines 4-68 and column 18, lines 1-59); and a plurality of buffers(314) having inputs receiving selected voltages and outputs that provide a plurality of gamma correction voltages(see figures 3, 12-13 and column 7, lines 44-59).

Kudo et al fail to disclose a tap resistor and an integrated circuit.

Kato teaches a multiple channel programmable gamma correction voltage generator comprising a tap resistor(20 or 40)(see figures 3, 5 and paragraphs 31-32 and 71) an integrated gamma correction circuit(see figure 2 and paragraph 28). It would have been obvious to have modified Kudo et al with the teaching of Kat, so as to reduce the number of connecting wires, ensure more stable correction and reduce the dimensions and weight of the LCD device(see paragraph 28).

As to claims 9 and 18, it would have been obvious to have a set of latches with an external load coupled to the memory device and providing the select values to the select logic since Kudo et al has disclosed an interface(907) with external load coupled to a memory device(301) and providing the select values to the select

logic(306, 308-313 or 1204 or 1205)(see figures 3, 9, 12-13; column 7, lines 33-43 and column 15, lines 2-25).

As to claim 10, Kudo et al teach memory device(301) stores a plurality of sets of select values, each corresponding to a different gamma correction value, and wherein the memory device(301) includes an address control input for selecting from among the plurality of sets of select values and loading the set of latches(figures 3, 9, 12-16; column 7, lines 44-68; column 8; column 17, lines 4-68 and column 18, lines 1-59);

As to claim 13, Kudo et al teach each of said M buffers(314)comprises an operational amplifier configured as a voltage follower(see figure 3 and column 7, lines 44-59).

As to claim 21, Kudo et al teach the imaging device comprises an LCD panel(see figures 3, 9 and column 14, lines 59-67).

As to claim 22, Kudo et al teaches control logic(906) coupled the memory(301) via address control, wherein the control logic(906) enables selection of a plurality of digital gamma values stored in the memory(301)(see figures 3, 9; column 7, lines 31-43 and column 15, lines 2-59).

3. Claims 2-4, 14-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable Kudo et al(7,023,458) in view of Kato(2002-0126112) and Suzuki et al(6,157,335).

As to claims 2-4, 14-15 and 17, Kudo et al as modified fail to disclose each of P-1 switch having a first terminal coupled to one of P-1 intermediate junctions.

Suzuki et al teach a circuit having an adjustable tap resistors(R3a-R3h) and

(P-1) switches(Sw1-SW8)(see figures 4, 8). Each of the (P-1) switch having a first terminal coupled to one of P-1 intermediate junctions(e.g. N1) (see figures 4, 8 and column 6, lines 20-58). It would have been obvious to have modified Kudo et al as modified with the teaching of Suzuki et al, so as to easy and accurate to select different resistance values and output voltages values(see column 2, lines 26-41).

As to claims 2 and 14, Kudo et al as modified by Suzuki et al teach a plurality of first resistors distributed along the resistor ladder, each coupled to a corresponding one of the plurality of adjustable tap resistors, each first resistor comprising: a plurality of second resistors(R3a-R3h), coupled in series forming a plurality of first junctions; and first switch logic(SW1-SW8) that inserts the corresponding one of the plurality of adjustable tap resistors at one of the plurality of first junctions(see Kudo's figures 3, 7 and Suzuki's figures 4, 8 and column 6, lines 20-58).

As to claim 14, Kudo teaches first switch logic(701) which inserts the corresponding one of the plurality of adjustable resistor at one of the plurality of first justions(see figures 3, 7A and column 13, lines 25-45).

As to claim 3, Suzuki et al teach select logic includes decoder logic(23) which closes one of the P-1(P is greater than 2) switches of each of the M(M is greater than 1) adjustable tap resistors to select each of the M tap voltages based on a corresponding one of M select values from the memory device(see figures 4 and column 6, lines 26-53).

As to claim 4, Kudo as modified by Suzuki teaches a decoder logic(23)comprises M decoders, each receiving a corresponding one of said M select

values and selecting a corresponding one of the P-1(P is greater than 2) switches of a corresponding one of the M adjustable tap resistors(see figures 4 and column 6, lines 26-58).

As to claim 15, Kudo et al as modified teach a plurality of adjustable tap resistors comprising a plurality of resistors(1R) coupled in series and forming a plurality of junctions and switch logic(704-706) selects one of plurality of junctions(see figures 3, 7A, 7B; column 13, lines 25-68 and column 14, lines 1-22).

As to claim 17, Kudo et al as modified by Suzuki et al teach each of the plurality of adjustable tap resistors comprises: a plurality of third resistors coupled in series and forming a plurality of second junctions; and second switch logic that selects one of said plurality of second junctions; and the select logic providing a gross adjustment to each said first switch logic and a fine adjustment to each the second switch logic(see Kudo's figures 3, 7 and Suzuki's figures 4, 8 and column 6, lines 20-58).

Allowable Subject Matter

4. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed on November 18, 2007 have been fully considered but they are not persuasive.

Applicants argue that Kudo does not teach selectively decoupling second resistors at corresponding intermediate locations and inserting corresponding adjustable tap resistors on page 10. However, the limitation of selectively decoupling second resistors at corresponding intermediate locations could not found anywhere in claim 1. Kudo teaches inserting corresponding adjustable resistors(see Kudo et al's figures 3, 7A-7B, 12 and column 13, lines 25-60) and Kato teaches a multiple channel programmable gamma correction voltage generator comprising a tap resistor(20 or 40)(see figures 3, 5, 12 and paragraphs 31-32 and 71). Thus, the combination of Kudo and Kato teach inserting corresponding adjustable tap resistors(see claim 1 rejection above).

Applicants argue that the cited reference doe not teach inserting adjustable tap resistors at selected intermediate location of a corresponding one of the plurality first resistors on page 11. The examiner disagrees with that since Kudo teaches inserting adjustable resistors(see figure 3 and 7) at selected intermediate location of a corresponding one of the plurality first resistors(326-330)(see figures 3, 7A-7B; column 7, lines 44-59 and column 13, lines 25-61). Kato teaches a multiple channel programmable gamma correction voltage generator comprising a tap resistor(20 or 40)(see figures 3, 5 and paragraphs 31-32 and 71). Thus, the combination of Kudo

and Kato teaches inserting adjustable tap resistors at selected intermediate location of a corresponding one of the plurality first resistors(see claim 1 rejection above).

Applicants argue that the cited references does not teach a plurality of first resistors distributed along a resistor ladder, each first resistor coupled to a corresponding one of a plurality of adjustable tap resistors, in which each first resistor comprising a plurality of second resistors coupled in series forming a plurality of first junctions, and the switch logic that inserts a corresponding one of the adjustable tap resistors at one of the first junctions on pages 11-12. The examiner disagrees with that since Kudo teaches a plurality of first resistors(326-330) distributed along a resistor ladder(307)(see Kudo's figures 3 and 12), each first resistor(326-330) coupled to a corresponding one of a plurality of adjustable resistors(see figures 3, 12; column 7, lines 44-59; column 11, lines 51-54 and column 17, lines 13-44) in which each first resistor(326-330) comprising a plurality of second resistors(308-313) coupled in series forming a plurality of first junctions, and the switch logic(701) that inserts a corresponding one of the adjustable resistors at one of the first junctions(see figures 3, 7, 12; column 13, lines 25-45 and claims 1 and 14 rejection above). Thus the combination of Kudo, Kato and Suzuki teaches all the limitation cited in claim 14(see claim 14 rejection above).

Applicants argue that Kudo as modified by Kato and Suzuki do not teach the limitation cited in claim 19 on page 13. The examiner disagrees with that since Kudo teaches a reference voltage(316) coupled across a resistor ladder(307) comprising a plurality of resistors(326-331) in series and forming a plurality of intermediate

junctions(see figures 3 and 12); plurality of potentiometers distributed along the resistor ladder(307) and providing a plurality of variable voltages(see figures 3, 7A-7B, 12; column 7, lines 44-68; column 8; column 9; column 10, lines 1-18 and column 13, lines 25-45) , wherein each of the plurality of potentiometers is inserted at a corresponding one of the plurality of intermediate junctions; a programmable non-volatile memory that stores at least one digital gamma value(see figures 3, 9, 12-16; column 7, lines 30-43; column 15, lines 7-68 and column 16, lines 1-12); select logic(304-306, 308-313 or 1204, 1205 or 1301-1306) , coupled to the memory and to the plurality of potentiometers, that selects from among the plurality of intermediate junctions for inserting the plurality of potentiometers and that selects each of the variable tap voltages according to the digital gamma value(see figures 7A-7B and column 13, lines 25-45); and a plurality of buffers(314) having inputs receiving selected tap voltages and outputs that provide said set of gamma corrected bias voltages(see figures 3, 12-13 and column 7, lines 44-59). Thus the combination of Kudo and Kato teaches all the limitation cited in claim 19(see claim 19 rejection above).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 20, 2008

Lun-yi Lao
Primary Examiner